Tutorial 5 - SS2016
Communication Systems and Protocols

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Task 1: Serial Interface

In the figure 1.1 the pulse diagram of a RS232 interface is given. Different transmission frames have been used for the communication. A transmission frame is composed of a start bit ('0'), 5-8 data bits, no (N, none) or one bit for even (E, even) or odd (O, odd) parity, as well as 1 or 2 stop bits (‚1'). Possible frame formats are [5..8][N,O,E][1,2], for example 8N1 for 8 data bits, no parity bit and at least 1 stop bit.

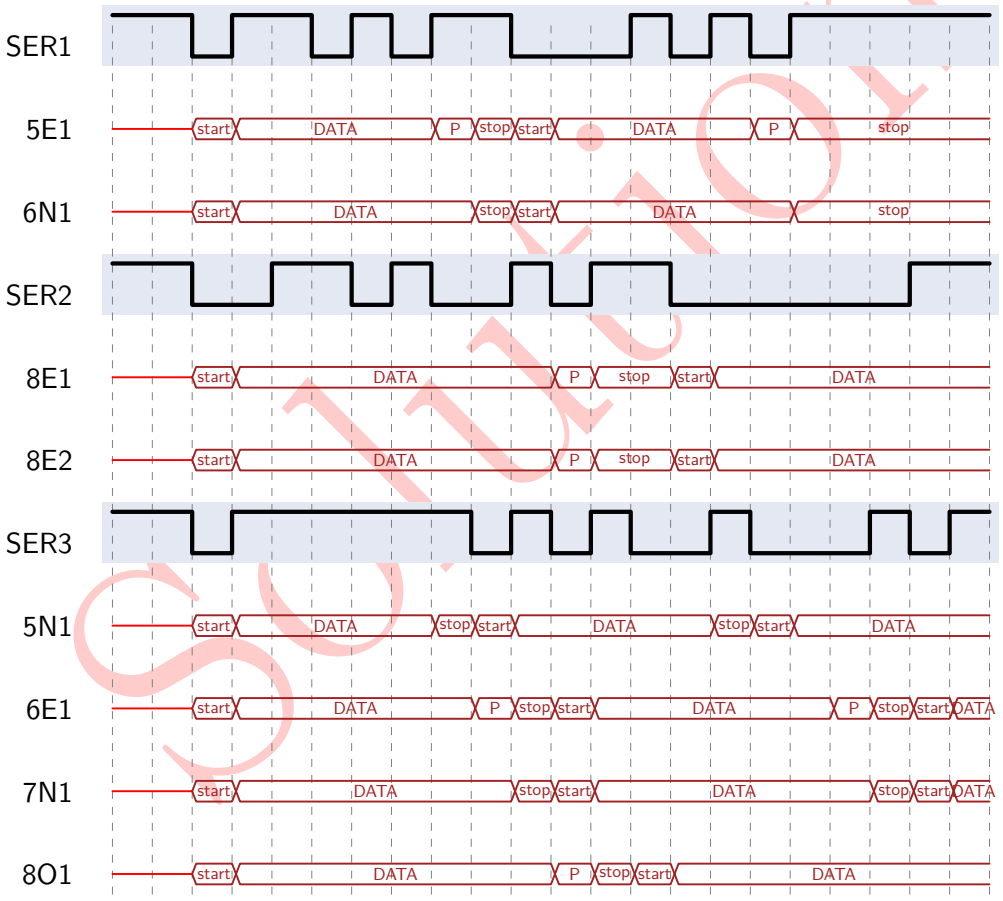

Figure 1.1: Serial interface pulse diagram

A) Give all possible frame formats for the pulse sequences as shown in figure 1.1. All given pulse sequences are describing a correct transmission. Start of a transmission is always the startbit in the third timestep.

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B) In the figure below different pulse sequences for a RS232 interface are given. Derive from the figure and the given frame formats if the transmission was error free. Mark the erroneous parts in the pulse diagrams. **2**

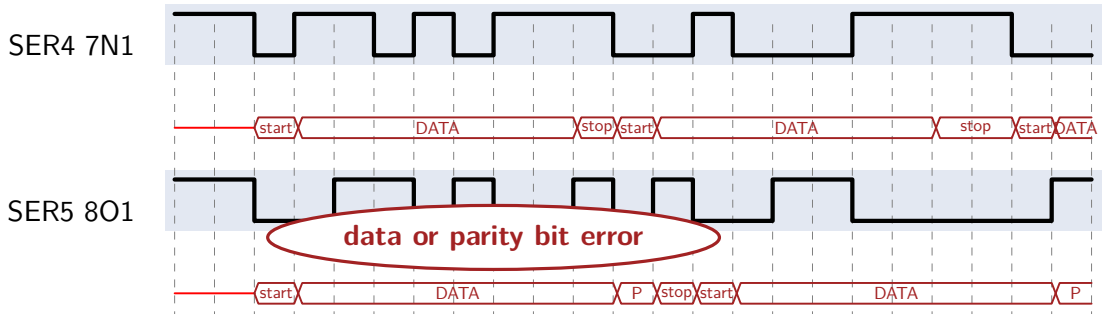

Figure 1.2: RS232 pulse sequences

C) Is it possible to detect errors without knowing the frame formats? **1**

c) Not in general. The frame format gives the position and meaning of a parity bit for example.

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Task 2: CAN Bus

Since CAN uses CSMA/CA as arbitration scheme every participant compares the actual bus level with the signal transmitted by itself. Because of that it is important for every participant to be able to evaluate the actual state on the bus before begin of a new bit. Here beside the signal runtime on the bus also the required processing time of the participant itself plays a role.

As given in Figure 2.1, this includes the processing time t_{CAN} of the CAN controller, the times t_{Rx} and t_{Tx} which are needed inside the transceiver for reception and transmission as well as the runtime t_{Bus} on the bus.

A) What is the interrelation between the maximum bus length and the bit transmission rate for CAN? Neglect the processing time inside the ECUs for this question **1**

Condition of simultaneity has to be fulfilled.
T_{Bit}: Duration for transmission of one bit
T_{Prop}: Signal runtime on the bus

Interrelation: $T_{Bit} >> T_{Prop}$

$\Rightarrow \frac{1}{TR} >> \frac{l}{v}$
TRTransmission rate, l Maximum bus length, v Velocity of propagation

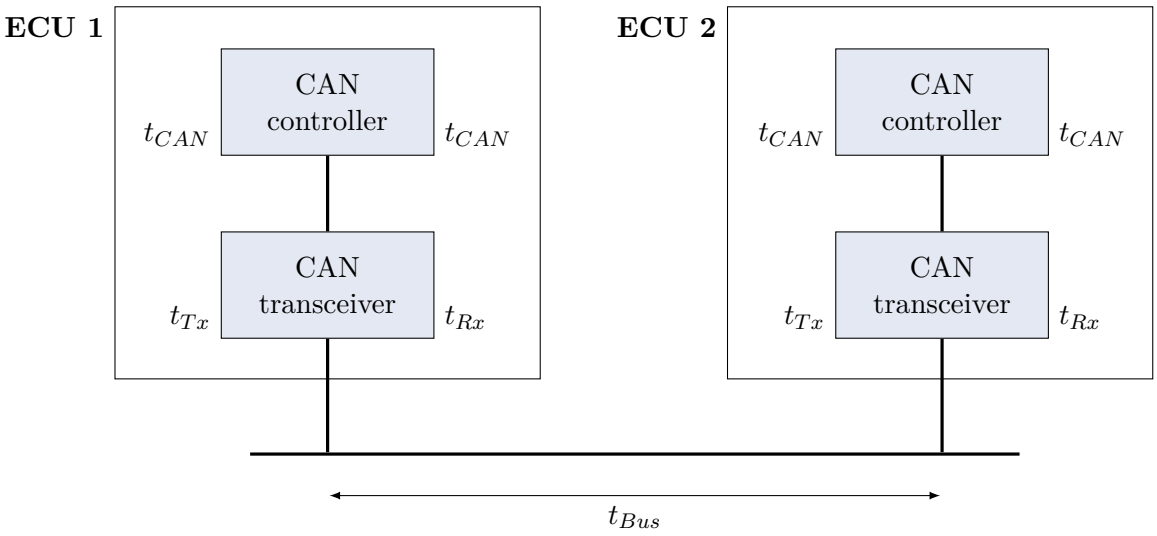

Figure 2.1: CAN bus

B) Based on the previous question, specify the maximum bus length for a speed of propagation of $v = 2.3 \cdot 10^8 m/s$ and for the transmission rates of $10 kbit/s$ and $1 Mbit/s$ respectively. **1**

First node to start an arbitration has to wait at least 2 times the duration for propagation of a signal on the bus until it gets a valid signal on the bus:

- One node starts arbitration. After 1x T_{Prop} the signal reaches the node at the end of the bus.
- Now this node knows that a new arbitration has started and sends out its own ID bit.
- The signals reaches the first node after another T_{Prop}. Now we have a stable value on the bus, 2x T_{Prop} after the first node started transmission.

$T_{Bit} \geq 2 \cdot T_{Prop} \Rightarrow l \leq \frac{v}{2 \cdot TR}$
For $10 kbits/s$: $l \leq \frac{2.3 \cdot 10^8 m/s}{2 \cdot 10 kbit/s} \Rightarrow l \leq 11500m$
For $1 Mbit/s$: $\Rightarrow l \leq 115m$

C) Now also consider the delays inside the ECUs. Which data transmission rate can be set as a maximum if the bus length between the two controllers that have furthest distance amounts to 300 meters? The detection of the bus state shall be accomplished after 80 percent of the bit time at latest (assume: $t_{CAN} = 75nsec$, $t_{Rx} = t_{Tx} = 25nsec$, $v_{Bus} = 0,2m/nsec$). **2**

Maximum transmission rate

Delay inside the participants:
$t_{TN} = 2 \cdot t_{CAN} + t_{Tx} + t_{Rx} = 2 \cdot 75ns + 2 \cdot 25ns = 200ns$
Delay on the bus:
$t_{Bus} = \frac{l_{Bus}}{v_{Bus}} = \frac{300m}{0.2m/ns} = 1500ns = 1.5\mu s$
Minimum bit duration:
$t_{Bit} \geq 2 \cdot (t_{TN} + t_{Bus}) = 2(0.2\mu s + 1.5\mu s) = 3.4\mu s$
Maximum transmission speed:
$S = \frac{1}{t_{Bit} * 0.8} = \frac{1}{3.4\mu s \cdot 0.8} = 368 Kbit/s$

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Task 3: PCI bus circle

Figure 3.1 shows the process of reading four data words within a burst on the PCI bus. The signals marked with "*" use negative logic. The FRAME* signal indicates the beginning and the end of a burst transaction. AD is the time multiplexed address- and data-bus. IRDY* (master) und TRDY* (slave) are used to insert waiting cycles after the transmission of an address. A waiting cycle is always inserted when at least one of the two signals is deactivated, that means it shows a high voltage level. All bus participants evaluate the state of a signal line at the rising edge of the clock. The clock frequency is 33.33MHz.

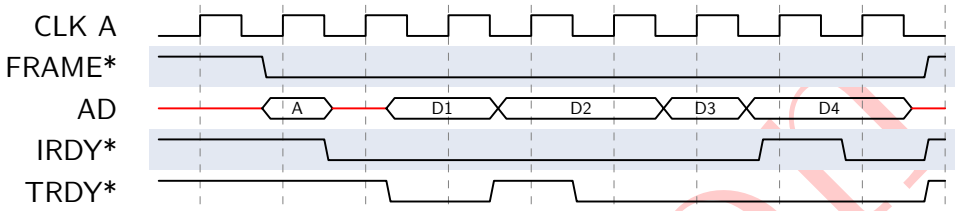

Figure 3.1: Simple PCI burst

A) How many waiting cycles are generated during the read burst given in Figure 3.1? 3

Criteria for a waiting cycle: After the address phase at least one of the signals IRDY* or TRDY* is HIGH.

- Cycle 2: IRDY* and TRDY* both are HIGH. Within this cycle the address is transmitted, so it is not a waiting cycle
- Cycle 3: TRDY* is HIGH → the target initiated the waiting cycle
- Cycle 5: TRDY* is HIGH → the target initiated the waiting cycle
- Cycle 8: IRDY* is HIGH → the initiator caused the waiting cycle

In total three waiting cycles are generated.

B) How long is the latency from the point in time when the activation of the FRAME* signal is detected by all bus participants to the point when the first data word can be read? 2

The FRAME* is recognized at the rising edge of cycle 2. The first data word is transmitted with the rising edge of cycle 4 since only then the slave signals the acceptance of the data by TRDY* = LOW.
The latency time results to: $2 \cdot \frac{1}{33.33MHz} = 2 \cdot 30ns = 60ns$

C) Assume that the address phase of a burst of infinite length has just ended and none of the involved participants forces waiting cycles. What is the data transfer rate of the PCI bus in this ideal case? (Approximation: $1MB = 10^6 Bytes$)

2

Width of the PCI bus: 32bit $\rightarrow$ 4 bytes per cycle
Duration of a cycle: $\frac{1}{33.33MHz} = 30ns$
Data transfer rate: $\frac{4Bytes}{30ns} = 133.33MBytes/s$

D) The time behavior of the PCI bus that can be seen in the picture is characteristic for a certain category of busses. What is the name of this category?

1

All signals are evaluated depending on the edge of a common clock signal $\rightarrow$ synchronous bus.

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Task 4: FireWire

A) FireWire uses a special coding scheme with an additional STROBE signal. Indicate the impulse diagram for the case that the following bit sequence (given in binary notation) should be transmitted. Use figure 4.1. 1

$$10011010001101111011110 0_b$$

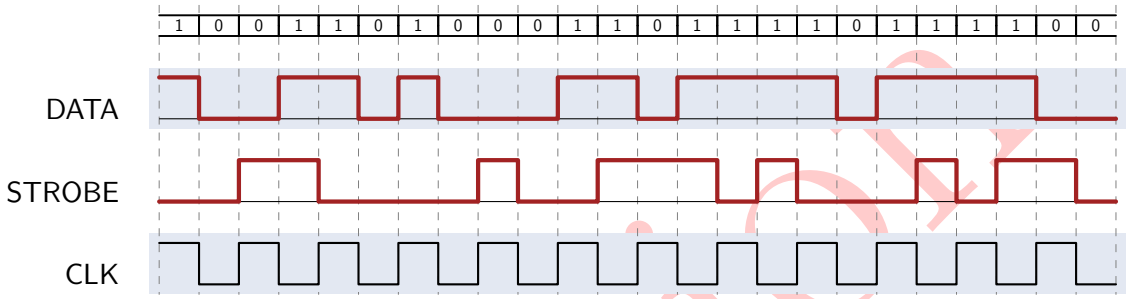


Figure 4.1: FireWire impulse diagram

Several FireWire devices are interconnected as shown in Figure 4.2.

B) Perform the three steps of address assignment for this network. Assume that every node needs one time unit for processing and forwarding of a message. Every node can process several incoming messages in parallel. In Figure 4.2 fill in the address that is obtained by every node. Which node becomes root of the tree? 3

The node with the adress 10 is the root of the network.

C) Now assume that the node highlighted in grey is not part of the network any more. What is the problem now during address assignment?
How could this problem be solved? 3

problem: Two nodes sending a parent request at the same time. Which node becomes root?
Solution: Random waiting time for the two remaining participants. After the waiting time a new notification message is transmitted. The participant that needs to wait for a longer time becomes root.

Task 4.1: FireWire structures

A) Different FireWire structures were built during a student laboratory. During test phase you notice that not all FireWire systems are working correctly. Please state if the FireWire systems given below are working correct. Mark the roots, if the systems are correct. Give a reason, if the FireWire system is not working correctly. 3

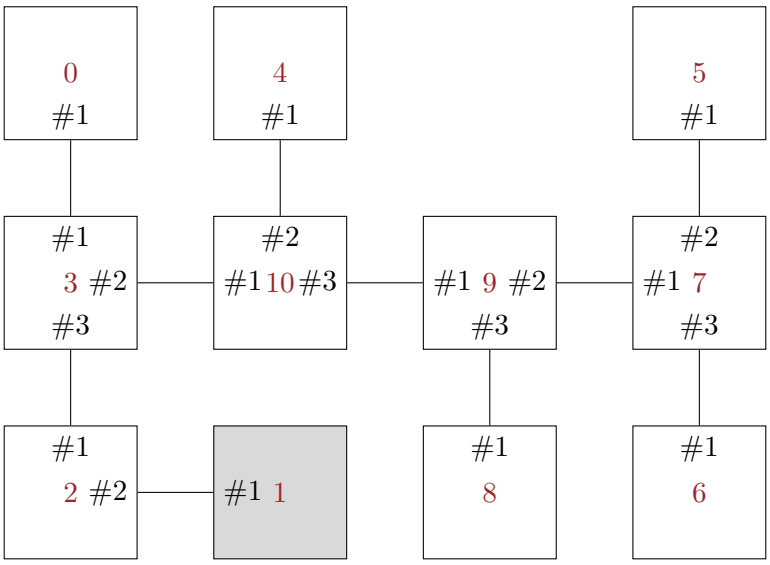


Figure 4.2: FireWire network

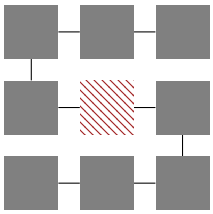
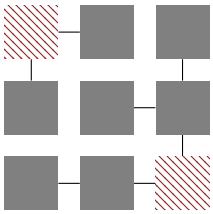
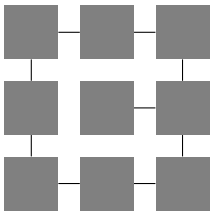
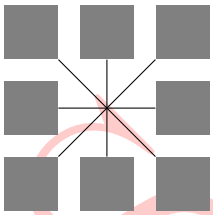
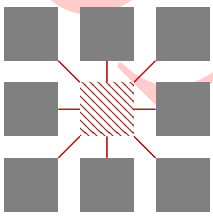
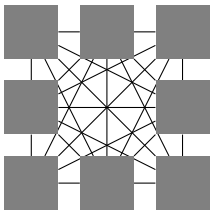
	Correct	Wrong	Reason
	x		
	x		
		x	Rings are not allowed in FireWire
		x	One output cannot have multiple connections
	x		
		x	Rings are note allowed in FireWire

Table 4.1: FireWire structures